OPTICAL ID IMAGE PROCESSOR

1. General Description

The SN9P700FG-201 is designed for implementing SONiX newly developed D.H.R.T. Technology (Data Hiding & Retrieving Technology), which integrates the solution that includes CMOS sensor interface, image recognizing engine and retrieved Optical ID output interface.

2. Product Spec. Summary

Voltage operation range: 3.0 ~ 3.3V (Reference design)

WirePower voltage operation range: 3.6 ~5.0V (Reference design)

Low power dissipation: 10mA (typ)

Embedded 16 bit-DSP for sensor control and image recognition

Light source timing Control

Built-in image recognizing engine

Embedded 16 bit-DSP for sensor control and image recognition

Up to 20 accurate optical index reports per second

Bi-directions communication in two wire serial interface

Output Optical Index in two wire serial interface

16MHz crystal and 3.3Volt only.

48 pin LQFP package.

3. DC Electrical Characteristics

a. Absolute maximum ratings

Symbol	Parameter	Rating	Units
Vcc	Power Supply	-0.3 to 3.6	V
Vin	Input Voltage	-0.3 to Vcc+0.3	V
Vout	Output Voltage	-0.3 to Vcc+0.3	V
Tstg	Storage Temperature	-55 to 150	°C

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b. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.0	3.3	3.6	V
Vin	Input voltage	0		Vcc	V
Topr	Operating Temperature	0		50	°C

c. DC electrical characteristics

(Under Recommended Operating Conditions and Vcc=3.0 ~ 3.6V , Tj=0 to +115 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input low voltage	LVTTL	-0.3		0.8	V
Vih	Input high voltage	LVTTL	2.0		Vcc+0.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	uA
Iih	Input high current	no pull-up or pull-down	-1		1	uA
Ioz	Tri-state leakage current		-1		1	uA
Vol	Output Low voltage	*			0.4	V
Voh	Output high voltage	*	2.4			V
Cin	Input capacitance			2.8		pF
Cout	Output capacitance		2.7		4.9	pF
Cbid	Bi-directional buffer Capacitance		2.7		4.9	pF

* : Maximum output current 4mA I/O pin .

4. Pin Assignment

Pin	Name	Type	Description
1	NC		Not connected
2	NC		Not connected
3	KEY1	I	Connected to 3.3V
4	GPIO0	I/O	This is the output to control Led status.
5	VDD	PWR	This is a 3.3V Supply Input for digital circuit.
6	GND	PWR	This is a return ground input for digital circuit.
7	GPIO1	I/O	This is I2C serial data line to EEPROM. It should be connected

			to Pin5 (SDA) of EEPROM.
8	GPIO2	I/O	This is I2C serial clock line to EEPROM. It should be connected to Pin6 (SCL) of EEPROM.
9	GPIO3	I	IR/RF wireless transmission mode control. This pin should be tied high in IR mode and should be tied low in RF mode.
10	RST	I	Enable chip reset when input is 3.3V
11	TEST_0	I	Connected to Ground
12	TEST_1	I	Connected to Ground
13	NC		Not connected
14	NC		Not connected
15	XVDD	PWR	This is a 3.3V Supply Input for oscillator(OSC)
16	XIN	I	This is OSC input. It should be connected to 16MHz OSC.
17	XOUT	I/O	This is OSC output. It should be connected to 16MHz OSC.
18	XVSS	PWR	This is a 3.3V Ground for oscillator(OSC)
19	GND	PWR	This is a return ground input for OSC.
20	VDD	PWR	This is a 3.3V Supply Input for digital circuit.
21	ADIO0	I/O	Not connected
22	ADIO2	I/O	Connected to ADO_SDIO line
23	NC		Not connected
24	NC		Not connected
25	NC		Not connected
26	VDD5D	PWR	This is a 3.3V~5.0V Supply Input for digital interface circuit.
27	ADIO1	I	Connected to ADO_SCK line
28	KEY0	I	Enable KEY0 function
29	PWR_EN	O	Enable Step down regulator
30	GND	PWR	This is a return ground input for digital circuit.
31	SEN_D0	I	This is Data0 input of SN9S100. It should be connected PinC3 (D0) of sensor
32	SEN_D1	I	This is Data1 input of SN9S100. It should be connected PinD3 (D1) of sensor.
33	VDD	PWR	This is a 3.3V Supply Input for analog circuit.
34	GND	PWR	This is a return ground input for digital circuit.
35	NC		Not connected
36	NC		Not connected

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37	NC		Not connected
38	NC		Not connected
39	SEN_CMD	I/O	Both sensor and Sonix SN9S100 Image Processor can transmit/receive data from the bus. It should be connected to Pin25 (SEN_CMD) of sensor.
40	SEN_CLK	O	This output signal to PinB4 (MCK) of sensor provides the clock to the sensor.
41	VSSA_IO	PWR	This is a return ground input for analog circuit.
42	VSSA_PEN	PWR	This is a return ground input for analog circuit.
43	IRED1	O	Connected to base of transistor1 to enable LED1
44	IRED_M1	I	for LED1 monitoring
45	IRED_M0	I	for LED0 monitoring
46	IRED0	O	Connected to base of transistor1 to enable LED0
47	VDDA_PEN	PWR	This is a 3.3V Supply Input for analog circuit.
48	VDD	PWR	This is a 3.3V Supply Input for digital circuit.

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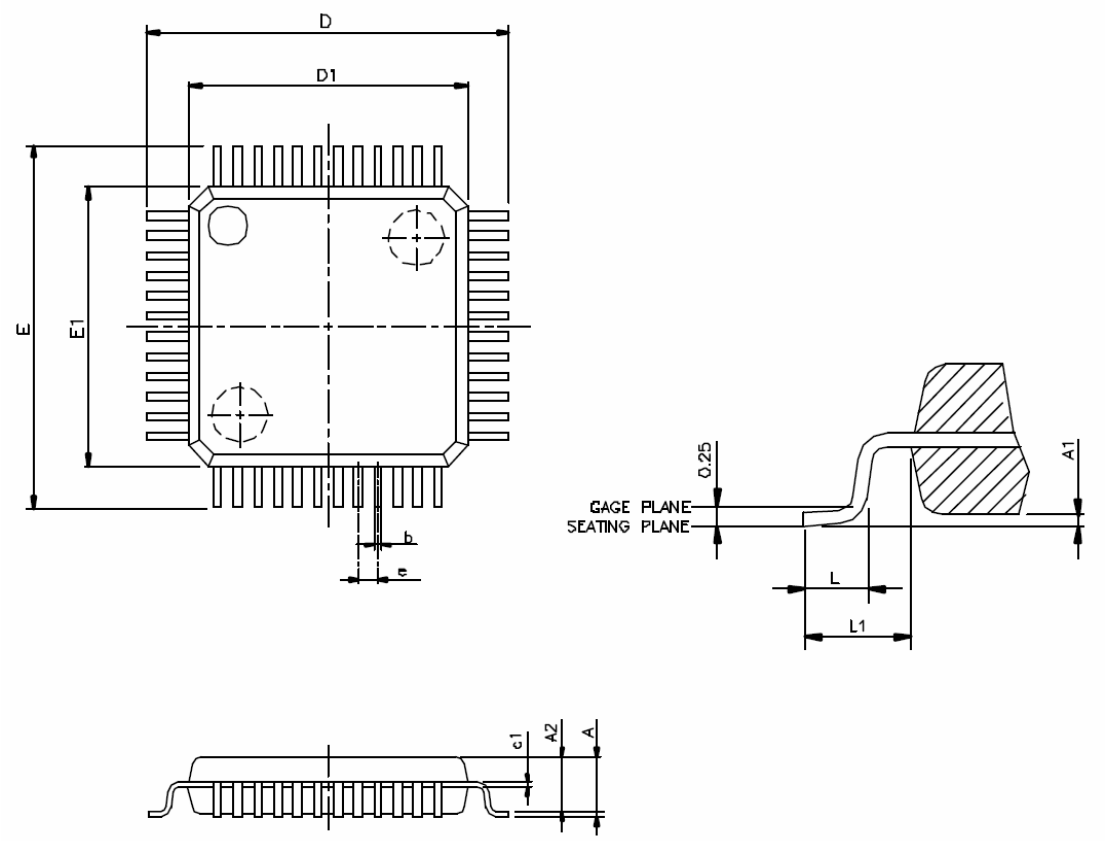
5. Package Information

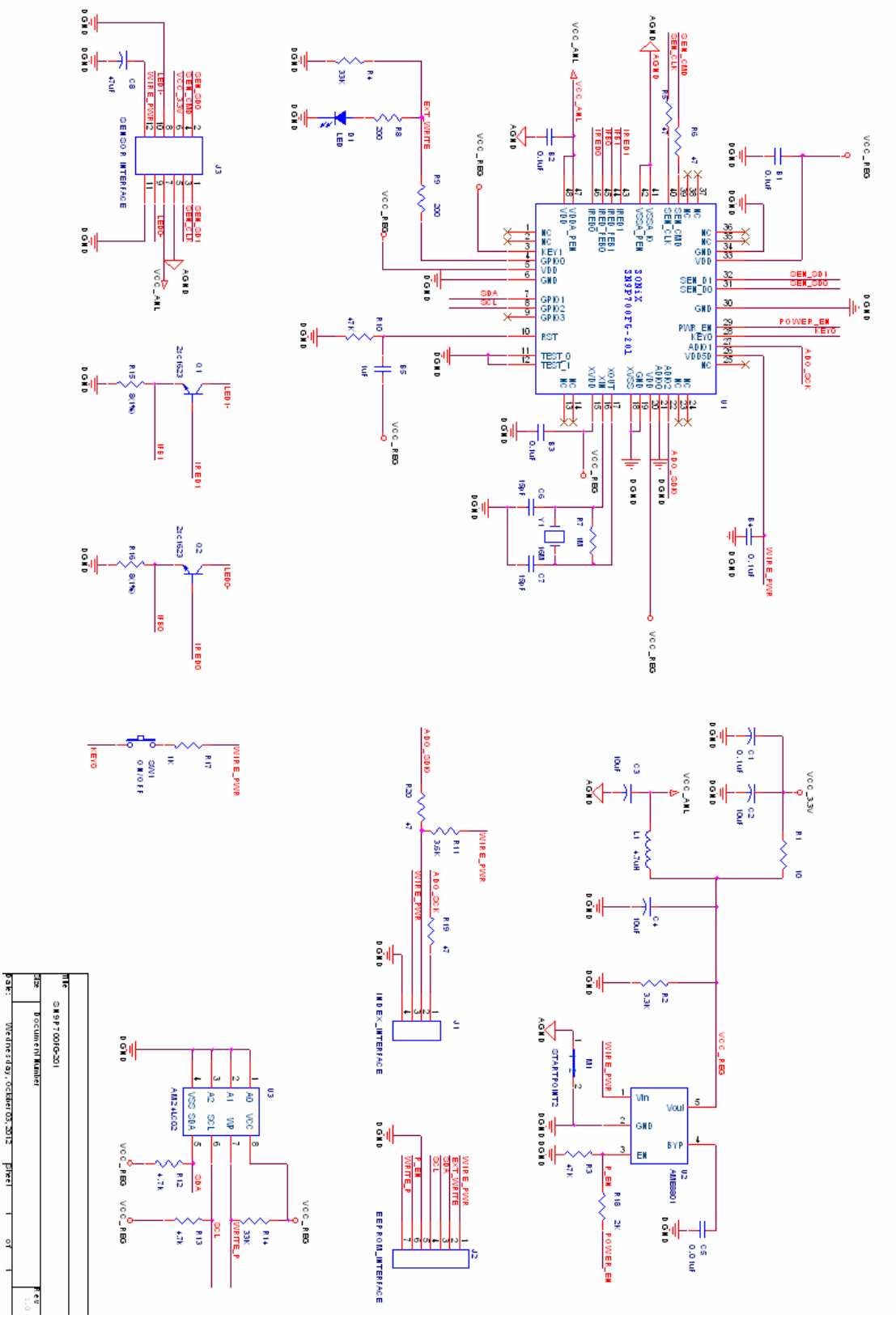


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.5 BSC	
b	0.17	0.27
L	0.45	0.75
L1	1 REF	

NOTES:
1.JEDEC OUTLINE:MS-026 BBC
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS IMCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

6. Reference Design



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